Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

1 (currently amended). A method for ~~encoding~~ storing data associated with a page within a non-volatile flash memory of a memory system, the page being the smallest unit of programming in the non-volatile flash memory, and having a data area and an overhead area, the method comprising:

dividing at least a part of the page into at least ~~two segments of the data, the at least two segments of the data including~~ a first segment and a second segment;

~~performing~~ encoding data associated with the first segment according to a first error correction code (ECC) ~~calculations on the first segment according to a first ECC~~ algorithm ~~to encode the first segment; and~~

encoding data associated with the second segment ~~performing error correction code (ECC) calculations on the second segment~~ according to a second ECC algorithm ~~to encode the second segment~~, wherein the data associated with the second segment is encoded substantially separately from the data associated with the first segment;

programming the page with the encoded data associated with the first and second segments.

2 (original). The method of claim 1 wherein the first segment includes the data area and the second segment includes the overhead area.

3 (original). The method of claim 1 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.

4 (previously presented). The method of claim 1 wherein the first ECC algorithm is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.

5 (original). The method of claim 4 wherein the first ECC algorithm is a Hamming Code ECC algorithm.

6 (original). The method of claim 1 wherein dividing the at least part of the page into the at least two segments of the data includes:

dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.

7 (previously presented). The method of claim 6 further including:

performing the ECC calculations on the third segment according to one of the first and second ECC algorithms to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.

8 (previously presented). The method of claim 6 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.

9 (original). The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.

10 (currently amended). The method of claim 1 wherein the non-volatile flash memory is one of a NAND flash memory and an MLC NAND flash memory.

11 (currently amended). A memory system comprising:

a non-volatile flash memory, the non-volatile flash memory including a page, the page being the smallest unit of programming in the non-volatile flash memory, and having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data;

code devices for dividing at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment;

code devices for ~~performing~~ encoding data associated with the first segment according to a first error correction code (ECC) ~~calculations according to a first ECC~~ algorithm ~~on the first segment to encode the first segment~~ and for encoding data associated with ~~on~~ the second segment according to a second ECC algorithm ~~to encode the second segment~~, wherein the data associated with the second segment is encoded substantially separately from the data associated with the first segment;

code devices for programming the page with the encoded data associated with the first and second segments; and

a memory area for storing the code devices.

12 (original). The memory system of claim 11 further including: a controller, the controller being arranged to process the code devices.

13 (original). The memory system of claim 11 wherein the first segment includes the data area and the second segment includes the overhead area.

14 (original). The memory system of claim 11 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.

15 (previously presented). The memory system of claim 11 wherein the first ECC algorithm is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.

16 (previously presented). The memory system of claim 15 wherein the first ECC algorithm is a Hamming Code ECC algorithm.

17 (original). The memory system of claim 11 wherein the code devices for dividing the at least part of the page into the at least two segments include:

code devices for dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.

18 (previously presented). The memory system of claim 17 further including:

code devices for performing the ECC calculations on the third segment according to one of the first and second ECC algorithms to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.

19 (previously presented). The memory system of claim 17 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.

20 (original). The memory system of claim 17 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.

21 (currently amended). The memory system of claim 11 wherein the non-volatile flash memory is one of a NAND flash memory and an MLC NAND flash memory.

22 (original). The memory system of claim 11 wherein the code devices are one of software code devices and firmware code devices.

23 (currently amended). A memory system comprising:

a non-volatile flash memory, the non-volatile flash memory including a page, the page being the smallest unit of programming in the non-volatile flash memory, and having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data;

means that divide at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; ~~and~~

means that ~~perform~~ encode data associated with the first segment according to a first error correction code (ECC) ~~calculations according to a first ECC~~ algorithm ~~on the first segment to encode the first segment~~ and that encode data associated with ~~on~~ the second segment according to a second ECC algorithm ~~to encode the second segment~~,

means for programming the page with the encoded data associated with the first and second segments; and

wherein the second segment is encoded substantially separately from the first segment.

24 (original). The memory system of claim 23 wherein the first segment includes the data area and the second segment includes the overhead area.

25 (original). The memory system of claim 23 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.

26 (canceled).

27 (original). The memory system of claim 23 wherein the means that divide the at least part of the page into the at least two segments include:

means that divide the page into three segments, the three segments including the first segment, the second segment, and a third segment.

28 (previously presented). The memory system of claim 27 further including:

means that perform the ECC calculations according to one of the first and second ECC algorithms on the third segment to encode the third segment,

wherein the third segment is encoded substantially separately from the first segment and the second segment.

29 (previously presented). The memory system of claim 27 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.

30 (original). The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.

31 (currently amended). The memory system of claim 23 wherein the non-volatile flash memory is one of a NAND flash memory and an MLC NAND flash memory.